GRAPE-4: A Special-Purpose Computer for Gravitational N-body problems

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Abstract

We describe GRAPE-4, a special-purpose computer for gravitational N-body simulations. In gravitational N-body simulations, almost all computing time is spent for the calculation of interaction between particles. GRAPE-4 (GRAPE stands for Gravity Pipe) is a specialized hardware to calculate the interaction between particles. It is used with a general-purpose frontend computer that performs all calculations other than the force calculation. With this architecture, it is relatively easy to realize a massively parallel system. In 1991, we developed the GRAPE-3 system with the peak speed equivalent to 14.4 Gflops. In 1992 we started the development of GRAPE-4. The GRAPE-4 system will consist of 1920 custom LSI chips. Each chip has the speed of 600 Mflops, when operated on 30 MHz clock. The sample chip was fabricated in August 1993, and we confirmed its normal operation on 50 MHz clock. The whole machine with the speed of 1.15 Tflops is scheduled to become operational by March 1995.

1 Introduction.

In this paper, we briefly overview the GRAPE-4 system, a special-purpose computer for gravitational N-body simulations. Many astrophysical objects are well approximated as a gravitational N-body system, in which point mass particles interact through gravity. The solar system, open clusters, globular clusters, galaxies, clusters of galaxies, and superclusters are all well expressed as gravitational N-body systems.

The N-body simulation is the most powerful tool to investigate the behavior of such gravitational N-body systems, since N-body problems with more than two particles have no general analytic solution. N-body simulations are, however, very expensive since the number of interaction is proportional to the square of the number of particles.

For some problems, it is possible to apply the particle-mesh (PM) algorithm to calculate the potential field and then calculate the force on each particles (see, *e.g.*, [1]). The PM scheme is fast because its calculation cost is $O(M \log M)$, where M is the number of grid points. However, there are many problems for which the PM scheme is not appropriate, since the spatial resolution of a PM scheme is limited by the grid size. For example, the simulation of the long-term evolution of globular clusters requires very accurate calculation of the interparticle force. Moreover, the number density and orbital timescale of stars range over many orders of magnitude in a single cluster. As a result, a fixed resolution of the PM scheme is not appropriate. The particle-particle particle-mesh (P^3M) scheme is not appropriate either, since the calculation cost of a grid cell with high density become very large. The tree algorithm does not help much, since the required accuracy of the force is high ([3],[2]).

For many problems, therefore, it is necessary to apply the straightforward algorithm, in which the gravitational force on a particle is calculated by summing up the contributions

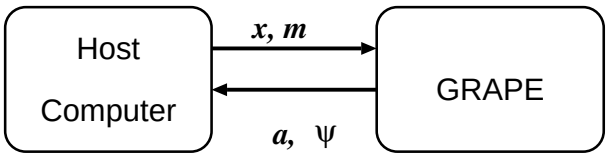

Figure 1: Basic structure of a GRAPE system

from all other $N-1$ particles in the system. This direct force calculation is well suited for acceleration by specialized hardware, because of the following two reasons. First, the force calculation itself is pretty simple. We calculate the difference in the positions of two particles $\Delta \mathbf{r}_{ij}$, and calculate the Newtonian gravitational force $-Gm_j \Delta \mathbf{r}_{ij}/|\Delta r_{ij}|^3$, where G is the gravitational constant and m_j is the mass of particle j. Total number of floating point operations involved is 17 plus one division and one square root operation. With the state-of-the-art VLSI technology, a fully hardwired pipeline to calculate the gravitational force can fit into one custom LSI chip. To build a hardwired pipeline from off-the-shelf LSI chips for floating-point operations is not very hard either.

Secondly, we can perform the rest of the calculation, such as the orbit integration of particles, on the general-purpose computer, provided that the communication between this host computer and the specialized hardware is not too slow.

Figure 1 shows the basic structure of a GRAPE system. The host computer sends the positions and the masses of particles. GRAPE hardware calculates the gravitational accelerations and the potential energy of particles and sends it back to the host computer.

The first machine we build, GRAPE-1 [4], had one pipeline that operated on a 8 MHz clock. Its theoretical peak speed was equivalent to 240 Mflops. GRAPE-1 used the number format with the accuracy lower than that of the standard floating point, in order to reduce the hardware cost. This decision resulted in short development time, but its application is rather limited due to the low accuracy. We build GRAPE-2 [5] and GRAPE-2A [6], which use the standard floating point format (partly double precision and partly single). Their peak speed was 40 and 180 Mflops, respectively. The force calculation pipelines of these machines are assembled with off-the-shelf LSI chips.

For GRAPE-3 [7], we implemented the force calculation pipeline in a custom LSI chip. We again used the low-accuracy number format similar to the format used in GRAPE-1, because the budget was severely limited. The original GRAPE-3 board had 24 custom chips and its speed was equivalent to 7.2 Gflops. We build two boards that worked in parallel. Thus the peak performance of the GRAPE-3 was 14.4 Gflops.

In year 1992, we started the development of GRAPE-4. It will consist of 40 processor boards. Each processor board houses 48 pipeline chips. Thus the total system consists of 1920 chips and its planned peak speed is 1.15 Tflops. In the rest of this paper, we describe the architecture of GRAPE-4 and present status of the project.

2 The architecture of GRAPE-4

Figure 2 shows the overview of the GRAPE-4 system. The GRAPE-4 system consists of a host computer and five clusters. One cluster has one host-interface board, one control board, and eight processor boards. We use a DEC Alpha workstation as the host computer. The host-interface board is connected to the host by TURBOchannel, DEC's own I/O bus. It's peak transfer rate is 100 MB/s, when DMA transfer is used. The host interface board and the control board are connected with 32bit parallel interface. Physical connection between them

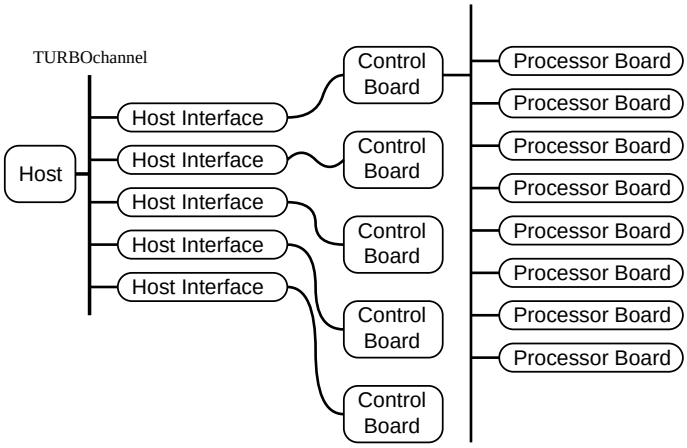

Figure 2: The GRAPE-4 system

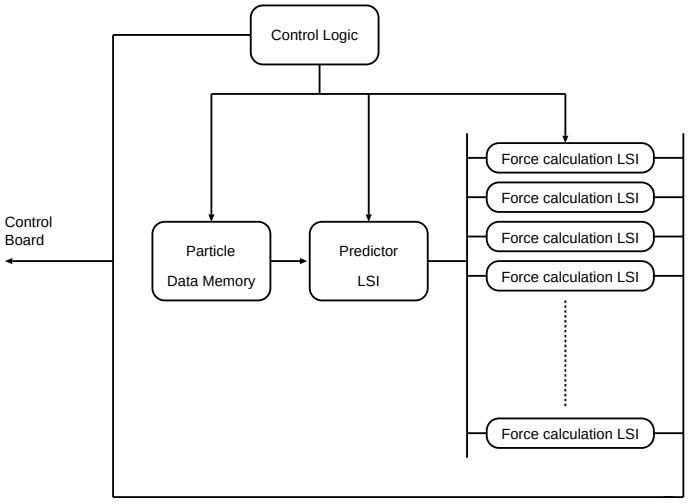

Figure 3: Processor board of GRAPE-4

is a coaxial flat cable. The control board and processor boards are connected by a backplane bus with 96 bit data width. A simple synchronous protocol is used on the backplane bus.

Figure 3 shows the structure of a processor board. The particle data memory stores the data of particles which exert the force. The predictor LSI is used to calculate the position (and velocity) of particles at a specified time. This function is necessary to use the individual timestep algorithm ([8], [9]). The force calculation LSI chips calculate the forces on particles. Each chip calculates the forces on two particles, using the "virtual multiple pipeline" (VMP). With VMP, the clock period of the pipeline LSI is two times as that of the system clock, and it calculates the forces on two different particles at alternate clock cycles. From the outside, one force calculation chip looks as if it has two pipelines. The advantage of this architecture is that we can increase the performance of the pipeline chip without increasing the system clock cycle. The predictor chip is a gate array and the pipeline chip is cell-based. Both are fabricated by LSI Logic Corp. The design rule is 1 μm and the gate count is about 50k and 100k for predictor and force calculation chips, respectively.

One board has 48 pipeline chips. These chips are packaged in an MCM (multi-chip module) package made by Kyocera. Thus one board has 6 MCM packages.

The control board has two main functions. The first one is to distribute the data received

from the host computer to processor boards. The second one is to sum up the calculated force and potential from processor boards. The summed result is transferred to the host computer through the host interface board. This summation process is necessary to reduce the bandwidth of the communication with the host computer [10].

The theoretical peak speed is 1.15 Tflops, for the system clock of 15 MHz and the pipeline clock of 30 MHz. Half of the peak speed will be achieved for the simulation of 5×10^4 particles.

3 Status of the Project.

We received the engineering samples of the custom chips in August 1993. We confirmed the normal operation of both chips with the system clock of up to 25 MHz. As of February 1994, we are debugging the host interface board and the control board. The prototype system will be operational by May 1994 and the whole system is scheduled to be operational by March 1995.

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